



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,982	10/18/2004	Juergen Pille	DE920030003US1	5981
24241	7590	01/10/2006	EXAMINER	
IBM MICROELECTRONICS INTELLECTUAL PROPERTY LAW 1000 RIVER STREET 972 E ESSEX JUNCTION, VT 05452			LE, THONG QUOC	
			ART UNIT	PAPER NUMBER
			2827	
DATE MAILED: 01/10/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

28

<b>Office Action Summary</b>	<b>Application No.</b> 10/711,982	<b>Applicant(s)</b> PILLE ET AL.	
	<b>Examiner</b> Thong Q. Le	<b>Art Unit</b> 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 20 October 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 11 is/are rejected.
- 7) ☒ Claim(s) 9 and 10 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Amendment filed on 10/20/2005 has been entered.
2. Claims 1-11 are presented for examination.

### ***Drawings***

3. The drawings were received on 10/20/2005. These drawings are acceptable.

### ***Response to Arguments***

4. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-8, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (U.S. Patent No. 5,672,987).

Regarding claim 8, Tanaka et al. disclose an integrated circuit memory array (Figure 1) adapted for low power operation, comprising:

a plurality of addressable memory cells (101, 100) arranged in rows and columns (Figure 1), the memory cells segmented into a plurality of memory blocks (Figure 1, 101);

a plurality of column lines (Figure 1, BL, XBL), each coupled to a corresponding column of memory cells;

a plurality of row lines (WL) , each coupled to a corresponding row of memory cells;

a precharge circuit (Figure 1, 105) coupled to the plurality of row lines, the precharge circuit provided to assert the plurality of row lines in a memory block to a high logic level following a memory access operation;

a first precharge signal controller (Figure 1, 112) coupled to the precharge circuit, the first precharge signal controller provided to generate a first precharge control signal (Figure 1, PRB);

a read cycle signal controller (Figure 1, 112) for generating a read cycle ( $n+1$ ) signal when a next memory access operation is read access operation (Figure 2, Column 5, lines 19-23) ; and

a logic element to evaluate the first precharge control signal and the read cycle control ( $n+1$ ) signal, the logic element asserting a second precharge when a next memory access is a read access for controlling the precharge circuit (Column 5, lines 19-23, lines 58-67, Column 6, 1-37, lines 58-67).

Regarding claim 11, Tanaka et al. disclose the memory array is SRAM (Column 1, lines 10).

Regarding claims 1-7, the apparatus discussed above would performed the method in claims 1-7 (Figure 3).

***Allowable Subject Matter***

7. Claims 8-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-9 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Tanaka et al. (U.S. Patent No. 5,672,987), and others, does not teach the claimed invention having a logic element comprises an AND gate, multiplexer as claims 8-9 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le  
Primary Examiner  
Art Unit 2827